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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,877	03/19/2004	William David Llewellyn	08211/0200389-US0/P05835	7655

38845 7590 04/03/2008

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EXAMINER	
KING, SONIA J	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
04/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,877	LLEWELLYN ET AL.	
	Examiner	Art Unit	
	Sonia J. King	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-20* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/21/2007 have been fully considered but they are not persuasive. The examiner is maintaining the previous rejection and provides the following responses to the applicant's arguments.

Claims 1-4, 6-8, 11, and 13-20

Applicant argues: Jackson fails to disclose, "the synthesized signal is a clock signal" as recited in Applicants' claim 1. The signal output by VCO 64 of Figure 3 of Jackson is a sinusoidal signal, not a clock signal.

The Examiner's response: It is well known in the art that a VCO in a PLL synthesizer is a clock signal. That is, the VCO in a phase locked loop or frequency synthesizer or PLL synthesizer is the output signal which acts as a clock signal. Also, a clock signal can be a sinusoidal signal. Therefore, claims 1, 13 and 20 and the dependent claims, 2-4, 6-8, 11 and 14-19 are not allowable.

Claims 9-10

Applicant argues: Claim 9 is respectfully submitted to be allowable at least because Jackson fails to disclose, teach, or suggest, "a clock divider circuit that is configured to provide an output clock signal from the synthesized signal", as recited in Applicant's claim 9.

The Examiner's response: Again, it is well known in the art that, the output signal from the VCO acts as a clock signal. Therefore, the clock divider circuit does provide an output clock signal.

Claim 12

Applicant argues: In Leung, frequency modulation is performed for reducing EMI. In Leung, the frequency modulation is done in a specific way to reduce EMI. In QPSK modulation, frequency modulation is performed to encode data. If Jackson were modified so that the frequency modulation was done in the manner taught in Leung, then the frequency modulation would no longer encode digital data. This is contrary to the purpose of the circuit of Jackson, which is to encode digital data by modulating the frequency. Accordingly, the proposed modification would render the circuit of Jackson unsuitable for its intended purpose.

The Examiner's response: The issue is not a matter of the circuit being operable or inoperable, since Leung is being used to fill the gap in order to solve the problem. Therefore, the issue that the applicant is arguing is one that is being presented now and not a matter that was previously presented.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 13 and 20 rejected under 35 U.S.C. 102 (b) as being anticipated by Jackson et al US PG Publication 2002/0067773 A1.

As to claim 1, Jackson et al discloses a spread spectrum clock generator that is arranged to provide an output clock signal, wherein the spread spectrum clock generator is arranged such that the output clock signal is a clock signal that is a spread-spectrum signal (Figure 3), and wherein the spread spectrum clock generator includes:

a phase detection circuit that is configures to provide an error signal from a reference signal and a feedback signal (Abstract); a voltage controlled oscillator circuit that is configured to provide a synthesized signal from the error signal (Abstract), wherein the synthesized signal is a clock signal, and wherein the output clock signal is based, at least in part, on the synthesized signal (Figure 3); a modulating waveform generator circuit that is configured to provide a modulating wave form signal that varies over time as a modulating waveform (Abstract); an accumulator circuit that is configured to provide a carry signal from the modulating waveform signal (Figure 3); and an adjustable clock divider circuit that is configured to provide an adjustable clock divider output signal from an adjustable clock divider input signal (paragraphs 0029 and 0030), wherein the adjustable clock divider input signal is based at least in part on the

synthesized signal paragraph 0031), the feedback signal is based at least in part on the adjustable clock divider output signal (paragraph 0031), and wherein the adjustable clock divider circuit is configured to provide the adjustable clock divider output signal such that a frequency that is associated with the adjustable clock divider signal corresponds to the frequency associated with the adjustable clock divider input signal divided by (paragraphs 0030, 0031): a first number, if the carry signal is associated with a first logic level (paragraph 0020), and a second number, if the carry signal is associated with a second logic level (paragraph 0032).

3. Claims 9 rejected under 35 U.S.C. 102 (b) as being anticipated by Jackson et al US PG Publication 2002/0067773 A1.

4. As to claim 9, Jackson et al teaches a phase detection circuit that is configures to provide an error signal from a reference signal and a feedback signal (Abstract); a voltage controlled oscillator circuit that is configured to provide a synthesized signal from the error signal (Abstract); a modulating waveform generator circuit that is configured to provide a modulating wave form signal that varies over time as a modulating waveform (Abstract); an accumulator circuit that is configured to provide a carry signal from the modulating waveform signal (Figure 3); and an adjustable clock divider circuit that is configured to provide an adjustable clock divider output signal from an adjustable clock divider input signal (paragraphs 0029 and 0030), wherein the adjustable clock divider input signal is based at least in part on the synthesized signal paragraph 0031), the feedback signal is based at least in part on the adjustable clock

divider output signal (paragraph 0031), and wherein the adjustable clock divider circuit is configured to provide the adjustable clock divider output signal such that a frequency that is associated with the adjustable clock divider signal corresponds to the frequency associated with the adjustable clock divider input signal divided by (paragraph 0030, 0031): a first number, if the carry signal is associated with a first logic level (paragraph 0020), and a second number, if the carry signal is associated with a second logic level (paragraph 0032) and a clock divider circuit that is configured to provide an output clock signal from the synthesized signal (Figure 1).

5. Claims 14 and 18 rejected under 35 U.S.C. 102 (b) as being anticipated by Jackson et al US PG Publication 2002/0067773 A1.

6. As to claim 14, Jackson et al teaches a clock divider circuit that is configured to provide the feedback signal from the synthesized signal (Figure 1).

7. As to claim 18, Jackson et al teaches a clock diver circuit that is configured to provide an output signal form the synthesized signal. (Figure 1)

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al US PG Publication 2002/0067773 A1 in view of Murkami US 4182988 A. As to claims 2 and 15, Jackson et al fails to teach wherein the second number equals the first number minus one. However, Murkami does teach this feature (Column 6 lines 40-43). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Jackson to include the frequency divider that teaches n/n-1 as taught by Murkami because if n/n+1 the opposite is also true.

10. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al in view of Jeon et al US PG Publication 2003/0058053 A1.

11. As to claim 3, Jackson et al fails to teach that the modulating waveform is suitable for reducing electromagnetic interference as claimed. However, Jeon et al does teach this feature in Figure 4. The advantage being that the phase locked-loop for reducing the EMI not only reduces the EMI, but also does not require a ROM. Thereby, the layout space can be reduced and broad frequency ranges can be obtained. Also, since the phase difference of the output signals of the VCO is controlled by logic circuits, the PLL is insensitive to changes in the manufacturing process. (Abstract)

12. Therefore, taking the combined teaching and Jeon as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the phase-locked loop circuit capable of adjusting the frequency range of spread spectrum clock as taught by Jeon so as to enable the whole system to be able to reduce the electromagnetic interference as in the claimed

invention. In so doing, a circuit that consumes less power, occupies a small layout space and can flexibly control a modulation frequency and a modulation rate flexibly is provided.

13. Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al as applied to claim 1 above, and further in view of Prockup US 6760571 B2.

14. As to claims 4 and 16, Jackson et al fails to teach a modulating waveform includes one of a triangle wave or a sinusoidal wave as in the claimed invention. However, Prockup does teach this feature in Figures 1, 2 and 3. Therefore, taking the combined teaching and Prockup as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the modulating waveform of a sine wave as taught by Prockup so that the whole modulation system can be accurately generated and measured well below a modulation frequency of 1Hz.

1. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al as applied to claim 1 above, and further in view of Watarai US PG Publication 2003/0053577 A1.

15. As to claim 6, Jackson et al fails to teach a charge pump and low-pass filter circuit. However, Watarai does teach this feature. In Watarai the phase control part has functions of phase detect, charge pump and low-pass filter. [paragraph 0028] Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Jackson to include the charge pump and low-pass filter because in

doing so the phase control variably controls the constant current source. (paragraph 0011)

16. As to claim 7, Jackson et al teaches a clock divider circuit that is configured to provide the adjustable clock diver input signal from the synthesized signal (Figure 3)

17. As to claims 8 and 17, Jackson et al teaches the modulating waveform signal includes a multiple-bit digital word that varies over time according to the modulating waveform (paragraph 0026)

18. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al, in view of Bickley US 5152005 A.

19. As to claims 10 and 19, Jackson fails to teach the clock divider circuit configured to provide the output signal such that a frequency that is associated with the output clock signal corresponds to a frequency that is associated with the synthesized signal divided by a third number as in the claimed invention. However, Bickley does teach this feature in Figure 3. Therefore, taking the combined teaching and Bickley as a whole, it would have been obvious to one of ordinary skill in the art at time of the invention to modify the combined teaching to include the synthesized signal divided by a third number as taught by Bickley such that a simple and inexpensive phase locked loop and frequency synthesizer circuitry could be provided. (Column 2 lines 45-51)

20.

Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al in view of Leung et al US 6580432 B1.

21. As to claim 11, Jackson et al fails to teach the modulating waveform is suitable for spreading a frequency spectrum that is associated with the synthesized signal relative to a frequency spectrum that is associated with the reference signal according to a downspread modulation. However, Leung does teach this feature. (Figure 1, Column 1 lines 50-57) Therefore, taking Jackson et al and Leung et al as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the downspread modulation as taught by Leung so that the entire system does not exceed the maximum processor's clock speed.

22. As to claim 12, Jackson et al teaches, a phase detection circuit that is configures to provide an error signal from a reference signal and a feedback signal (Abstract); a voltage controlled oscillator circuit that is configured to provide a synthesized signal from the error signal (Abstract); a modulating waveform generator circuit that is configured to provide a modulating wave form signal that varies over time as a modulating waveform (Abstract); an accumulator circuit that is configured to provide a carry signal from the modulating waveform signal (Figure 3); and an adjustable clock divider circuit that is configured to provide an adjustable clock divider output signal from an adjustable clock divider input signal (paragraphs 0029 and 0030), wherein the adjustable clock divider input signal is based at least in part on the synthesized signal paragraph 0031), the feedback signal is based at least in part on the adjustable clock divider output signal (paragraph 0031), and wherein the adjustable clock divider circuit is configured to provide the adjustable clock divider output signal such that a frequency

that is associated with the adjustable clock divider signal corresponds to the frequency associated with the adjustable clock divider input signal divided by (paragraph 0030, 0031): a first number, if the carry signal is associated with a first logic level (paragraph 0020), and a second number, if the carry signal is associated with a second logic level (paragraph 0032). Jackson et al fails to teach wherein the modulating waveform is suitable for spreading a frequency spectrum that is associated with the synthesized signal relative to a frequency spectrum that is associated with the reference signal according to a down-spread modulation, and wherein the down-spread modulation is between approximately -.5% to -1.5%, as in the claimed invention. However, Leung does teach this feature (Figure 1, Column 1lines 50-57) Therefore, taking Jackson et al and Leung et al as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include the downspread modulation as taught by Leung so that the entire system does not exceed the maximum processor's clock speed.

Allowable Subject Matter

23. Claim 5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sonia J. King whose telephone number is 571-270-1307. The examiner can normally be reached on Mon-Fri 7:30am-5pm alt Fri's off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sonia J. King/
Examiner, Art Unit 2611

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